REMARKS

As a RCE is being filed herewith, it is requested that the finality of the rejections be withdrawn, and this amendment entered in the above-identified application. Additionally, Applicants are submitting herewith an Information Disclosure Statement. It is respectfully requested that this new Information Disclosure Statement be considered with the further examination of this application.

The claims of the present application are directed to a method of manufacturing a semiconductor device. As explained on page 2, lns. 5-15, one of the most important criteria in evaluating a TFT of a semiconductor device is the reliability of the device. One of the most significant problems effecting reliability is the presence of contaminating impurities, such as alkaline metals and alkaline earth metals, in the interface between the semiconductor film and the gate insulating film or in the interface between the gate insulating film and the gate wiring. An example of these problems with reliability is shown in Figs. 4-6 and on page 4, ln. 5 - page 5, ln.1 of the specification where sodium (Na) exists in the interface between a gate wiring and a gate insulating film.

The claimed method of the present application is intended to improve the reliability of the resulting semiconductor device by removing the contaminating impurities from a first film before forming a second film thereover. In particular, independent Claims 11, 15 and 19 include the step of removing contaminating impurities from a surface of a semiconductor film or island by spin etching before forming a gate insulating film over the semiconductor film or island. The spin etching is recited in these claims as the following steps:

> "spinning the substrate;
> contacting an etching solution to a surface of said semiconductor (film or island) and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface; and then".

The method of independent Claims 23 and 27 also addresses the reliability problem with contaminants by removing contaminating impurities from a surface of a gate wiring by spin etching before forming a gate insulating film and a semiconductor film. In particular, these claims recite the steps of

> "spinning the substrate;
> contacting an etching solution to surfaces of said substrate and said gate wirings and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surfaces; and then"

As explained below, none of cited references disclose or suggest these steps.

Each of the Examiner's objections/rejections will now be addressed in the order they appear in the Final Rejection.

Claim Rejections - 35 USC §102

In the Final Rejection, the Examiner rejects Claims 11-14 under 35 USC §102(b) as being anticipated by Belscher et al. This rejection is respectfully traversed as Belscher does not disclose or suggest the claimed invention.

As explained above, amended independent Claim 11 recites steps for spin etching to remove any contaminating impurities from the surface of the semiconductor film. There appears to be no disclosure or suggestion in Belscher of such steps. Hence, independent Claim 11 and those claims dependent thereon are patentable over this reference, and it is respectfully requested that the rejection be withdrawn.

Claim Rejections - 35 USC §103

The Examiner also rejects Claims 15-30 under 35 USC §103 as being unpatentable over

Kobayashi et al. in view of Mautz et al.[1] This rejection is also traversed.

As the Examiner admits, Kobayashi does not disclose or suggest the spin etching steps to remove contaminating impurities recited in the claims in the present application.

As a result, the Examiner cites Mautz. However, Mautz discloses a process wherein a first interlayer insulating layer 28 is formed over a source region 22, a drain region 23 and a gate electrode 25. Col. 3, lns. 50-64; Fig. 2. A drain opening 291 and a gate contact opening 292 are then formed in layer 28 and plugs formed therein. Col. 3, ln. 60- col. 2, ln. 5; Fig. 3. An interconnecting layer 41 and photoresists 421 and 422 are then formed over layer 28 and plugs. Col. 4, lns. 8-10; Fig. 4. Etching is then done to form drain interconnect 411 and gate interconnect 412. Col. 4, lns. 31-34; Fig. 5. After the etching and removal of the photoresists, layer 28 and interconnects 411 and 412 are rinsed. Col. 5, lns. 23-34.

Mautz does not disclose or suggest the steps of the claimed method of the present application. Hence, even if Kodayashi and Mautz were combined (which Applicants do not agree is proper), the combination still fails to disclose or suggest the claimed steps of removing contaminating impurities from a surface of a semiconductor film/island by spin etching before forming a gate insulating film as required in independent Claims 11, 15 and 19, or removing contaminating impurities from surfaces of a semiconductor film/island and a gate wiring by spin etching before forming a gate insulating film as required in independent Claims 23 and 27.

Therefore, the claims of the present application are patentable over the cited references and should now be allowed.

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[1] In the Final Rejection, the Examiner states that Applicant did not traverse the rejection of claims 19-23. Applicants have reviewed their prior response, and note that while the comments therein were general, it was Applicants' intention to traverse the rejection of all the claims, including Claims 19-23. In this response, Applicants again traverse the Examiner's rejection of all the claims, including Claims 19-23.

Please charge Deposit Account No. 50-1039 for any fee for this submission.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

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Marked-up copy of the claims as amended:

IN THE CLAIMS:

Please amend the claims as follows:

11. (Amended) A method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film formed over a substrate;

[removing a contaminating impurity from the surface of the semiconductor film; and]

spinning the substrate;

contacting an etching solution to a surface of said semiconductor film and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface; and then

forming a gate insulating film in contact with the semiconductor film from the surface of which the contaminating impurity has been removed.

15. (Amended) A method of manufacturing a semiconductor device, comprising steps of:

forming at least one semiconductor island over a substrate;

spinning the substrate [by using a spinning apparatus];

contacting an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface; and then

forming a gate insulating film over said semiconductor island.

19. (Amended) A method of manufacturing a semiconductor device, comprising steps of:

forming a semiconductor film over a substrate;

crystallizing said semiconductor film;

forming at least one semiconductor island over said substrate by patterning the crystallized semiconductor film ;

spinning the substrate [by using a spinning apparatus];

contacting an etching solution to a surface of said semiconductor island and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surface; and then

forming a gate insulating film over said semiconductor island; and

forming a gate electrode over said gate insulating film.

23. (Amended) A method of manufacturing a semiconductor device, comprising steps of:

forming gate wirings over a substrate;

spinning the substrate [by using a spinning apparatus];

contacting an etching solution to surfaces of said substrate and said gate wirings and scattering the etching solution during said spinning, thereby contaminating impurities are removed from the surfaces; and then

forming a gate insulating film and a semiconductor film over said gate wirings.

27. (Amended) A method of manufacturing a semiconductor device, comprising steps of:

forming gate wirings over a substrate;

spinning the substrate [by using a spinning apparatus];

contacting an etching solution to surfaces of said substrate and said gate wirings and scattering the etching solution during said spinning, thereby contaminating impurities are removed

from the surfaces; and then

forming a gate insulating film and a semiconductor film over said gate wirings, continuously.